IN THE CLAIMS:

The following is a current listing of claims and will replace all prior versions and listings of claims in the application. Please amend the claims as follows:

Claims 1-133 (Cancelled).

134. (Previously Presented) A semiconductor device, comprising:

a memory transistor having a composite gate structure containing a first conductive film, a first insulating film, and a second conductive film that overlie a first channel region, wherein said first conductive film is disposed closer to said first channel region than said second conductive film; and

a peripheral transistor having a single gate structure containing a third conductive film and a fourth conductive film that overlie a second channel region and are in contact over their cross-sections, wherein said third conductive film is disposed closer to said second channel region than said fourth conductive film;

wherein said second, third, and fourth conductive films each have a conductivity that is substantially the same and that is higher than a conductivity of said first conductive film.

135. (Cancelled).

136. (Previously Presented) The semiconductor device of claim 134, wherein said first conductive film and said third conductive film have substantially the same thickness.

137. (Previously Presented) The semiconductor device of claim 136, wherein said second conductive film and said fourth conductive film have substantially the same thickness.

138. (Previously Presented) The semiconductor device of claim 137, wherein said second conductive film, said third conductive film, and said fourth conductive film have an impurity concentration that is substantially the same and that is at least 10 times an impurity concentration of said first conductive film.

139-141. (Cancelled).

142. (Previously Presented) The semiconductor device of claim 134, wherein an impurity concentration of said first conductive film is between $1x10^{18}$ and $1x10^{19}$ atoms/cm^3.

143. (Previously Presented) The semiconductor device of claim 142, wherein an impurity concentration of said third conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.

144. (Previously Presented) The semiconductor device of claim 143, wherein an impurity concentration of said second conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.

145. (Previously Presented) The semiconductor device of claim 144, wherein an impurity concentration of said fourth conductive film is between $1x10^{20}$ and $1x10^{21}$ atoms/cm^3.

146-151. (Cancelled).

152. (Previously Presented) The semiconductor device of claim 134, wherein said first, second, third, and fourth conductive films are polycrystalline silicon films.

153. (Previously Presented) The semiconductor device of claim 134, wherein said first insulating film is a silicon oxide/silicon nitride/silicon oxide (ONO) film.

154. (Previously Presented) The semiconductor device of claim 134, wherein said first conductive film is doped with phosphorous.

155. (Previously Presented) The semiconductor device of claim 134, wherein said first conductive film is doped with arsenic.

156. (Previously Presented) The semiconductor device of claim 134, wherein the semiconductor device is an EEPROM.

157. (Previously Presented) The semiconductor device of claim 134, wherein the semiconductor device is an EPROM.

158. (Previously Presented) The semiconductor device of claim 134, wherein said second, third, and fourth conductive films have substantially the same resistance.

159-169. (Canceled).

170. (Previously Presented) A semiconductor device, comprising:

a memory transistor having a composite gate structure containing a first conductive film, a first insulating film, and a second conductive film that overlie a substrate, wherein said first conductive film is separated from said substrate by a tunnel oxide layer, and wherein said first conductive film is separated from said second conductive film by said first insulating film; and

a peripheral transistor having a single gate structure containing a third conductive film and a third conductive film that overlie said substrate, wherein said fourth conductive film is on top of said third conductive film, and wherein said third and fourth conductive films are in contact over their cross-sections;

wherein said second, third, and fourth conductive films each have a conductivity that is substantially the same and that is higher than a conductivity of said first conductive film.

171. (Previously Presented) The semiconductor device of claim 170, wherein a gate oxide film and a field oxide film are between said substrate and said third conductive film.

172. (Previously Presented) The semiconductor device of claim 170, wherein said second conductive film, said third conductive film, and said fourth conductive film have an impurity concentration that is substantially the same and that is at least 10 times an impurity concentration of said first conductive film.